(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 938 094 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
25.08.1999 Bulletin 1999/34

(51) Int. Cl.[6]: **G11C 7/00**

(21) Application number: **99101209.7**

(22) Date of filing: **22.01.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **19.02.1998 JP 3734898**
27.02.1998 JP 4758798
27.02.1998 JP 4758898
25.08.1998 JP 23906298

(71) Applicant:
Sanyo Electric Co., Ltd.
Moriguchi-shi, Osaka 570-0083 (JP)

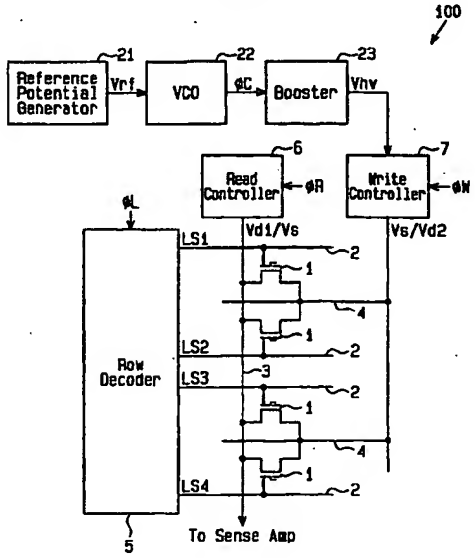
(72) Inventors:
- **Hasegawa, Kazuhiro**
  Anpachi-gun, Gifu-ken 503-0116 (JP)
- **Yoneyama, Akira**
  Ora-gun, Gunma-ken 370-0518 (JP)

(74) Representative:
Geyer, Werner, Dr.-Ing. et al
Patentanwälte
Geyer, Fehners & Partner
Perhamerstrasse 31
80687 München (DE)

(54) Write circuit for a semiconductor memory device

(57) A write circuit supplies a write potential that is higher than a power supply potential to memory cells (1) of a semiconductor memory device. The write circuit includes a reference potential generator (21) that generates a reference potential having a substantially constant potential difference from one of a power supply potential and a ground potential. A voltage-controlled oscillator (VCO) (22) connected to the reference potential generator receives the reference potential and generates an oscillation clock signal in proportion to the reference potential. A booster (23) connected to the VCO generates the write potential by piling up the oscillation clock signal onto the power supply potential in a multistage manner. A write controller (7) is connected to the booster and supplies the write potential to the memory cells in accordance with a write clock.

Fig.2



EP 0 938 094 A1

[0013] Briefly stated, the present invention provides a write circuit for supplying a write potential that is higher than a power supply potential to memory cells of a semiconductor memory device. The device includes a reference potential generator that generates a reference potential having a substantially constant potential difference from one of a power supply potential and a ground potential. A voltage-controlled oscillator (VCO) connected to the reference potential generator receives the reference potential and generating an oscillation clock signal having an oscillation clock frequency in proportion to the reference potential. A booster connected to the VCO that generates a write potential by piling up the oscillation clock signal onto the power supply potential in a multistage manner. A write controller is connected to the booster and supplies the write potential to the memory cells in accordance with a write clock.

[0014] The present invention provides a method of generating a write potential that is higher than a power supply potential to memory cells of a semiconductor memory device. First, a reference potential is generated that has a substantially constant potential difference from one of a power supply potential and a ground potential. Then, an oscillation clock signal having an oscillation clock frequency is generated in proportion to the reference potential. A write potential is generated by piling up the oscillation clock signal onto the power supply potential in a multistage manner. Then, the write potential is supplied to the memory cells in accordance with a write clock.

[0015] Other aspects and advantages of the invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

[0016] The invention, and preferred objects and advantages thereof, may best be understood by reference to the following description of the certain exemplifying embodiments together the accompanying drawings in which:

FIG. 1 is a schematic block diagram of a conventional nonvolatile semiconductor memory device.
FIG. 2 is a schematic block diagram of a nonvolatile semiconductor memory device according to a first embodiment of the present invention.
FIG. 3 is a circuit diagram of a write circuit for the memory device of FIG. 2.
FIG. 4 is a schematic block diagram of a nonvolatile semiconductor memory device according to a second embodiment of the present invention.
FIG. 5 is a circuit diagram of a write circuit of the memory device of FIG. 4.
FIG. 6 is a schematic block diagram of a nonvolatile memory device according to a third embodiment of the present invention.
FIG. 7 is a circuit diagram of the write circuit of the memory device of FIG. 6.

[0017] In the drawings, like numerals are used for like elements throughout.

(First Embodiment)

[0018] FIG. 2 is a schematic block diagram of a nonvolatile semiconductor memory device 100 according to a first embodiment of the present invention. The nonvolatile semiconductor memory device 100 is equipped with the memory cell transistors 1, the word lines 2, the bit line 3, the source lines 4, the row decoder 5, the read controller 6, the write controller 7, a reference potential generator 21, a voltage-controlled oscillator (VCO) 22, and a booster 23.

[0019] The reference potential generator 21 generates a reference potential Vrf and supplies the reference potential Vrf to the voltage-controlled oscillator (VCO) 22. The reference potential Vrf always has a constant potential difference from the ground potential or power supply potential.

[0020] The voltage-controlled oscillator (VCO) 22 is preferably a ring oscillator having a negative feedback loop, and varies the frequency of an oscillation clock signal ϕc by fluctuating the delay time of the negative feedback loop in response to the reference potential Vrf.

[0021] The booster 23 generates the high potential Vhv that is higher than the power supply potential by laying or piling up the waveform of the oscillation clock signal ϕc from the VCO 22 onto the power supply potential in a multistage manner and supplies the high potential Vhv to the write controller 7. The write controller 7 supplies the high potential Vhv to the source line 4 as the write potential Vd2 in accordance with the write clock signal ϕw.

[0022] Because the reference potential Vrf maintains a substantially constant potential difference from and the power supply potential or ground potential, the VCO 22 generates the oscillation clock signal ϕc having a constant or substantially constant frequency. The booster 23 generates the high potential Vhv in accordance with the oscillation clock signal ϕc. In other words, the current supply capacity of the booster 23 is determined according to the frequency of the oscillation clock signal ϕc. Accordingly, while the reference potential Vrf is maintained at the predetermined level, a substantially constant write current flows in the memory cell transistor 1. In other words, the operation of writing information to the memory cell transistor 1 is made stable by the write controller 7.

[0023] FIG. 3 is a circuit diagram illustrating the reference potential generator 21, the VCO 22, and the booster 23 of FIG. 2.

[0024] The reference potential generator 21 is equipped with a resistor 31, an N-channel type MOS transistor 32, a P-channel type MOS transistor 33, and an N-channel type MOS transistor 34. The resistor 31 and the transistor 32 are connected in series between the power supply potential and ground potential, and a

voltage of the breakdown voltage of the diode 54 and the threshold voltage of the transistor 55, current flows into the ground through the diode 54 and the transistor 55. Accordingly, the high potential Vhv is limited to the predetermined potential.

[0034] The write controller 7 receives the high potential Vhv from the booster 23 and applies the write potential Vd2 to the selected memory cell transistor 1. Thus, the constant write potential Vd2 is applied to the selected memory cell transistor 1 and the constant current flows to the selected memory cell.

(Second Embodiment)

[0035] FIG. 4 is a schematic block diagram of a nonvolatile semiconductor memory device 200 according to a second embodiment of the present invention. The nonvolatile semiconductor memory device 200 is equipped with the memory cell transistors 1, the word lines 2, the bit line 3, the source lines 4, the row decoder 5, the read controller 6, the write controller 7, the VCO 22, the booster 23, a level shift circuit 24, and a reference potential generator 25.

[0036] The reference potential generator 25 generates a reference potential Vrf having a substantially constant potential difference from the ground potential or power supply potential and supplies the reference voltage Vrf to the voltage-controlled oscillator 22. The reference potential generator 25 changes or corrects the reference potential Vrf in accordance with an intermediate potential Vmv supplied from the level shift circuit 24 described below.

[0037] The level shift circuit 24 receives the high potential Vhv from the booster 23 and shifts the level of the high potential Vhv to a level that is lower than the power supply potential to generate the intermediate potential Vmv. In other words, the level shift circuit 24 generates the intermediate potential Vmv that follows the fluctuation of the high potential Vhv and supplies intermediate potential Vmn to the reference potential generator 21.

[0038] The level of the high potential Vhv drops if the current supply capacity of the booster 23 is insufficient. In other words, when the level of the high potential Vhv drops, the reference potential generator 21 feeds back and controls the VCO 22 so that the frequency of the oscillation clock signal ϕc increases based on the intermediate potential Vmn. This feedback control maintains the level of the high potential Vhv substantially constant.

[0039] FIG. 5 is a circuit diagram of the VCO 22, the booster 23, the level shift circuit 24, and the reference potential generator 25 of FIG. 4.

[0040] The reference potential generator 25 is equipped with P-channel type MOS transistors 71 and 72 and N-channel type MOS transistors 73 and 74. The transistors 71 and 73 are connected in series between the power supply potential and ground potential and the intermediate potential Vmv from the level-shift circuit 24 is applied to the gate of the transistor 73. The gate of the transistor 71 is connected to a node N3 between the transistors 71 and 73. The first reference potential Vrp is output from the node N3. The transistors 72 and 74 are connected in series between the power supply potential and ground potential, and the gate of the transistor 72 is connected to the node N3. The gate of the transistor 74 is connected to a node N4 between the transistors 72 and 74. The second reference potential Vrn is output from the node N4.

[0041] The level shift circuit 24 is equipped with two resistors 61 and 62 and an N-channel type MOS transistor 63. The resistors 61 and 62 and the transistor 63 are connected in series between the power supply potential and ground potential, and the high potential Vhv from the booster 23 is applied to the gate of the transistor 63. The intermediate potential Vmv is output from a node N5 between the resistors 61 and 62. The transistor 63 has a high-dielectric strength structure. Accordingly, even if the high potential Vhv is applied to the gate, no current leakage is generated. The resistances of the resistors 61 and 62 are set so that the intermediate potential Vmv between the ground potential and power supply potential is obtained in accordance with the high potential Vhv applied to the gate of the transistor 63.

[0042] In the level shift circuit 24, when the level of the high potential Vhv drops, the intermediate potential Vmv rises. In the reference potential generator 25, in accordance with the rise of the intermediate potential Vmv, the first reference potential Vrp drops and the second reference potential Vrn rises. Thus, the delay time of each inverter 40 in the VCO 22 is decreased. Accordingly, the frequencies of the oscillation clock signal ϕc and inverse clock signal $*\phi c$ increase and as a result, the current supply capacity of the booster 23 improves. Thus, the level of the high potential Vhv generated by the booster 23 is corrected.

(Third Embodiment)

[0043] FIG. 6 is a schematic block diagram of a nonvolatile semiconductor memory device 300 according to a third embodiment of the present invention. The nonvolatile semiconductor memory device 300 is equipped with the memory cell transistors 1, the word lines 2, the bit line 3, the source lines 4, the row decoder 5, the read controller 6, the write controller 7, the reference potential generator 21, the VCO 22, the level shift circuit 24, and a booster 26.

[0044] The booster 26 receives the intermediate potential Vmv from the level shift circuit 24 and sets the initial potential based on the intermediate potential. The booster 26 lays the peak value of the oscillation clock signal ϕc onto the initial potential and generates the high potential Vhv. In other words, when the level of the high potential Vhv drops and the intermediate potential Vmv rises, the booster 26 is designed so that the initial

tial in accordance with the intermediate potential.

5. The write circuit of claim 4, **characterized in that** said reference potential generator (25) includes a pair of transistors (71,73) connected in series between the power supply potential and ground potential, the intermediate potential is applied to the gate of one of the pair of transistors, and the reference potential is output from a node between the pair of the transistors.

6. The write circuit of claim 1 or 3, **characterized by** a level shift circuit (24) connected to said booster (26), for shifting the level of the write potential to a lower level than the power supply potential to generate an intermediate potential, said booster generating the write potential based on the intermediate potential.

7. The write circuit of claim 6, **characterized by** said voltage-controlled oscillator (22) generates the oscillation clock signal and an inverse clock signal that is the inverse of the oscillation clock signal, said booster (26) includes a plurality of series connected first transistors including odd and even transistors (82a-82d), a plurality of capacitors including odd and even capacitors (83a-83d), and a second transistor (81), the odd stage capacitors (83a,83b) have a first terminal connected to the gate and the drain of the odd stage first transistors (82a,82c) and a second terminal that receives the oscillation clock signal, the even stage capacitors (83b,83d) have a first terminal connected to the gate and the drain of the even stage first transistors (82b,82d) and a second terminal that receives the inverse clock signal, and the second transistor (51) has its gate connected between the power supply potential and the first stage first transistor (82a), for receiving the intermediate potential.

8. The write circuit of claim 7, **characterized in that** said reference potential generator (21) includes:

a resistor (31) having a first end connected to the power supply potential and a second end;
a first transistor (32) connected between said resistor second end and a ground potential, wherein a gate of the first transistor is connected to a first node N1 between the resistor and the first transistor; and
a pair of transistors (33,34) connected in series between the power supply potential and the ground potential, wherein a second node N2 between the transistor pair is connected to a gate of a first one of the pair of transistors and a gate of the second one of the pair of transistors is connected to the gate of the first transistor, and wherein a potential between said resistor and said first transistor is output at the first node N1 as a first reference potential and a potential between the transistor pair at the second node N2 is output as a second reference potential.

9. The write circuit of one of claims 1 to 3, **characterized in that** said reference potential generator (21) includes:

a resistor (31) having a first end connected to the power supply potential and a second end;
a first transistor (32) connected between said resistor second end and a ground potential, wherein a gate of the first transistor is connected to a first node N1 between the resistor and the first transistor; and
a pair of transistors (33,34) connected in series between the power supply potential and the ground potential, wherein a second node N2 between the transistor pair is connected to a gate of a first one of the pair of transistors and a gate of the second one of the pair of transistors is connected to the gate of the first transistor, and wherein a potential between the resistor and the first transistor is output at the first node N1 as a first reference potential and a potential between the transistor pair at the second node N2 is output as a second reference potential.

Fig.2

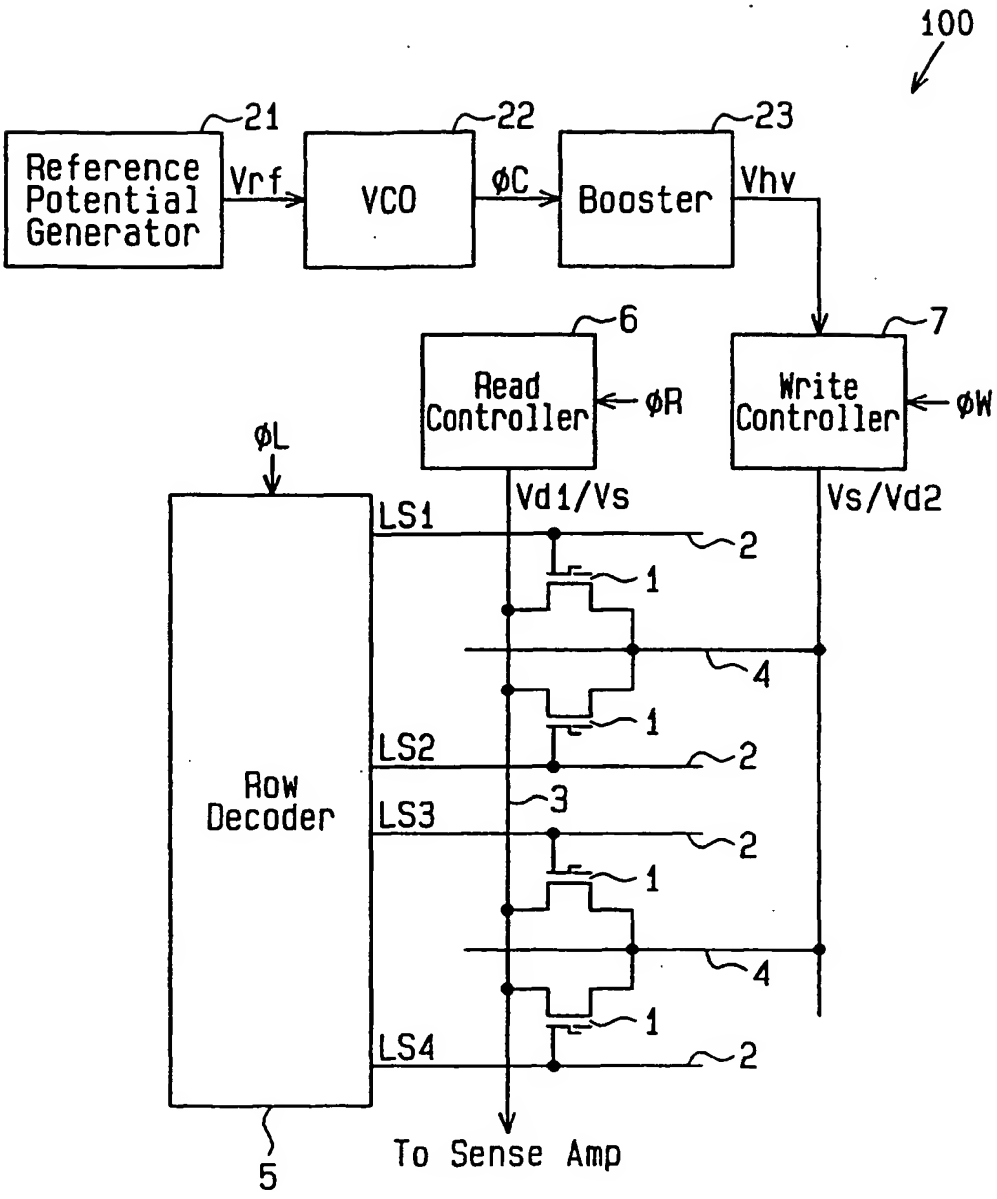

100
21
Reference Potential Generator
Vrf
22
VCO
φC
23
Booster
Vhv
6
Read Controller
φR
7
Write Controller
φW
φL
Vd1/Vs
Vs/Vd2
LS1
LS2
LS3
LS4
Row Decoder
1
2
3
4
5
To Sense Amp

Fig.4

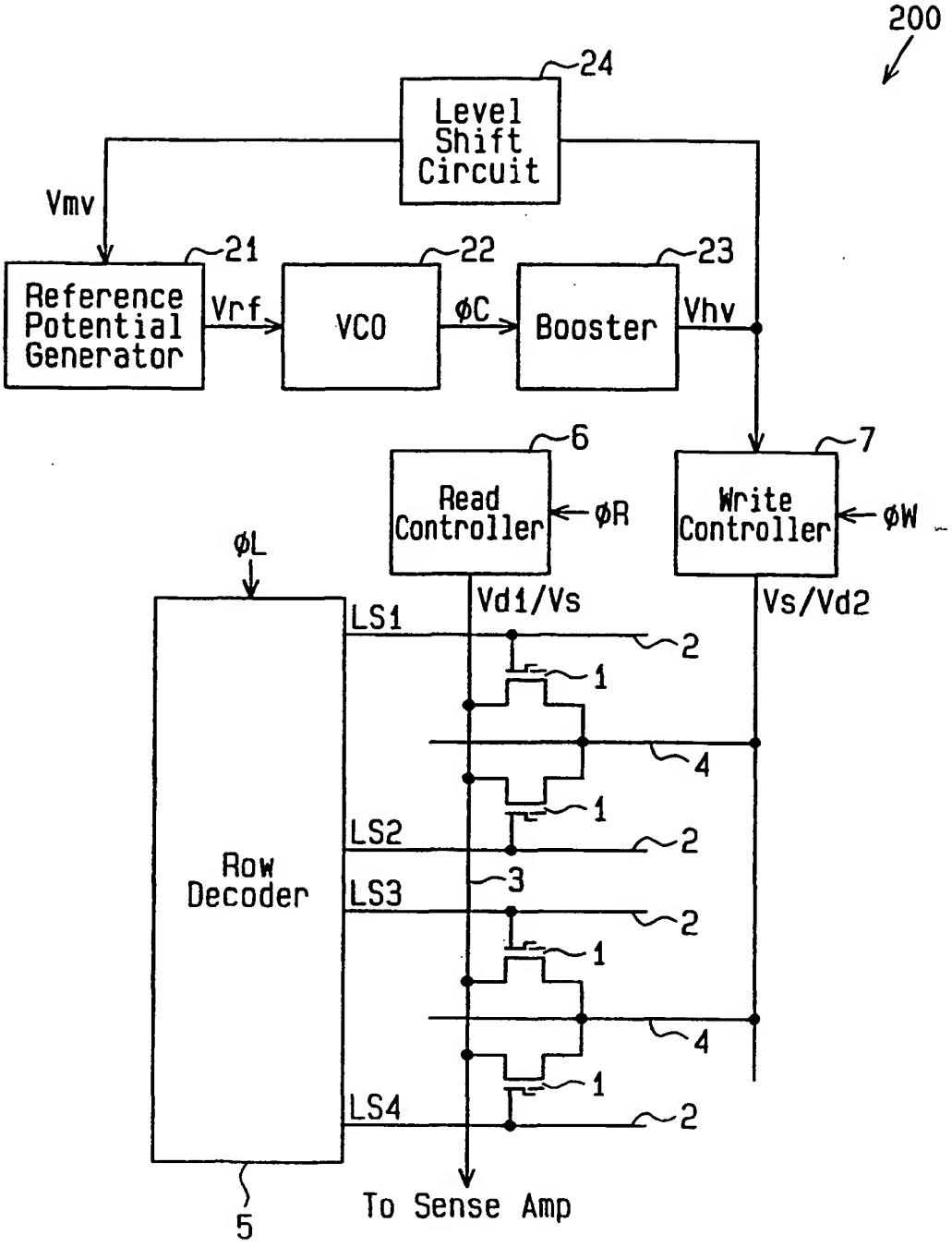
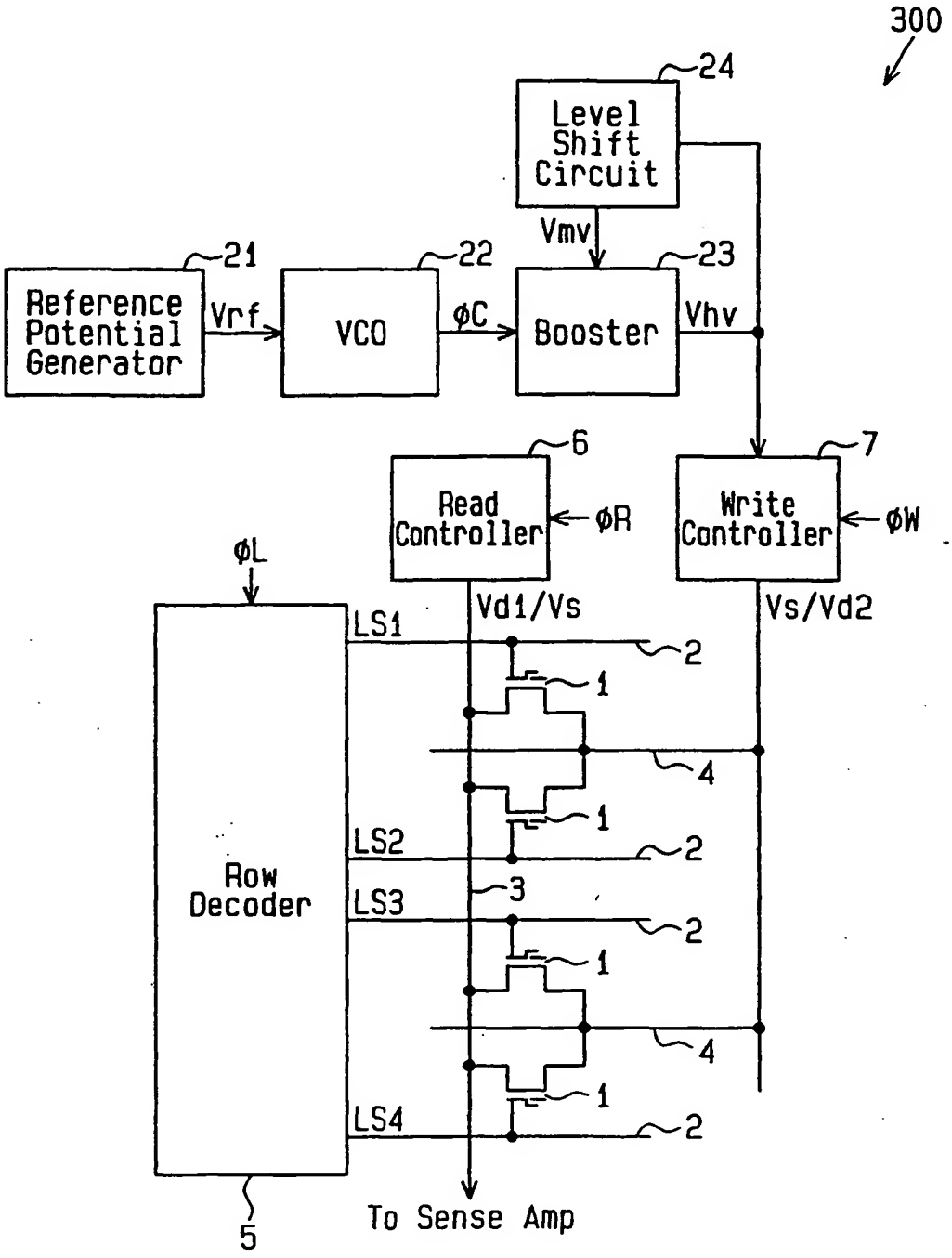

200
24
Level Shift Circuit
Vmv
21
Reference Potential Generator
Vrf
22
VCO
φC
23
Booster
Vhv
6
Read Controller
φR
7
Write Controller
φW
φL
Vd1/Vs
Vs/Vd2
LS1
LS2
LS3
LS4
Row Decoder
1
2
3
4
5
To Sense Amp

Fig.6


300
24
Level Shift Circuit
Vmv
21
22
23
Reference Potential Generator
Vrf
VCO
φC
Booster
Vhv
6
7
Read Controller
φR
Write Controller
φW
φL
Vd1/Vs
Vs/Vd2
LS1
LS2
LS3
LS4
Row Decoder
1
2
3
4
5
To Sense Amp

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 99101209.7

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 6)
A	US 5661686 A (GOTOU, H.) 26 August 1997 (26.08.97), abstract, column 1, line 5 - column 4, line 26, claim 1, fig. 1. --	1	G 11 C 7/00
A	US 5615146 A (GOTOU, H.) 25 March 1997 (25.03.97), abstract, column 1, line 5 - column 3, line 43, claim 1, fig. 1. --	1	
A	EP 0710959 A2 (NEC CORP.) 08 May 1996 (08.05.96). ----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl. 6)
			G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	06-05-1999	GRÖSSING

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons.

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0001)